THE CHIP-SCALE ATOMIC CLOCK – PROTOTYPE EVALUATION

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Abstract

The authors have developed a chip-scale atomic clock (CSAC) for applications requiring atomic timing accuracy in portable battery-powered applications. At PTTI/FCS 2005, we reported on the demonstration of a prototype CSAC, with an overall size of 10 cm^3, power consumption ≈150 mW, and short-term stability $\sigma_y(\tau)<1x10^{-9}\tau^{-1/2}$. Since that report, we have completed the development of the CSAC, including provision for autonomous lock acquisition and a calibrated output at 10.0 MHz, in addition to modifications to the physics package and system architecture to improve performance and manufacturability.

Ten pre-production CSACs have been constructed in order to test unit-to-unit performance variations and to gain statistical confidence in operating specifications, environmental sensitivity, and manufacturability. All of the units have been subjected to a standard set of performance tests. Several of the units have been distributed to DoD system integrators and external testing facilities. Others have been subjected to environmental testing, including shock and vibration, long-term aging, and temperature performance.

This paper will review the CSAC architecture, with particular attention to those aspects which have evolved since our previous report, as well as the results of evaluation of the pre-production CSACs.

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INTRODUCTION

The authors have developed a chip-scale atomic clock (CSAC) for deployment in applications requiring atomic timing in portable battery-powered instruments. The CSAC occupies a unique niche in the spectrum of timing sources. It is nearly two orders of magnitude smaller and lower power than a conventional rubidium oscillator (Rb) and roughly one order of magnitude larger and higher power than a temperature-compensated crystal oscillator (TCXO). The stability and environmental sensitivity of the CSAC is somewhat inferior to Rb, but far superior to a TCXO. The CSAC enables new capabilities for DoD systems in secure communications, navigation, friend-or-foe identification, and ad-hoc networking, as well as commercial applications requiring precise timing in GPS-denied environments.

The realization of the CSAC has been the result of a highly successful collaboration between the Research group at the Symmetricom Technology Realization Center, the MEMs group at The Charles Stark Draper Laboratory, and the Optoelectronics Division of Sandia National Laboratories. Throughout the CSAC development program, Symmetricom has provided periodic status updates to the PTTI community via presentations at the annual PTTI Meeting **[1-4]**.

Since our last PTTI update, at the Joint PTTI/FCS conference in 2005, the Symmetricom-led team has completed the development of a first-generation CSAC, suitable for field-testing in prospective applications. For programmatic reasons, the previous and current CSAC designs are designated "Phase-II" and "Phase III," respectively, reflecting the phases of the DARPA CSAC program under which this development was accomplished. We have built 10 pre-production Phase-III units for the purposes of evaluating unit-to-unit variability and to distribute to systems engineers for applications demonstrations.

CSAC ARCHITECTURE

The CSAC architecture has been described in detail in previous PTTI reports, particularly **[3]** and **[4]**. While the Phase-II CSAC described in our 2005 PTTI report provided an important proof-of-concept demonstration, further development was necessary in order to create a field-deployable autonomous device. In particular:

1) The short-term stability of $\sigma_y(\tau) \approx 5x10^{-10}\ \tau^{-1/2}$ lacked adequate margin to consistently achieve the program objective of $\sigma_y(\tau) < 6x10^{-10}\ \tau^{-1/2}$.
2) The cost of the physics package was unacceptably high, due to the relatively high cost of the integrated VCSEL/Photodetector optoelectronic component.
3) The digital tuning resolution was relatively coarse, $\Delta y \approx +/-10^{-8}$/step.
4) The device did not acquire lock automatically, requiring a skilled operator and specialized equipment to perform the power-on sequence.
5) The output frequency was highly sensitive to temperature fluctuations, $dy/dT \approx 10^{-10}$/°C.
6) The long-term stability (drift) was relatively poor due to aging of the physics package.

Recent development activity has addressed these deficiencies. The Phase-III physics package architecture has been evolved from the "folded-optics" design of **[3]** to a more conventional "through-path" design, which leads to improved short-term stability and significant reduction in the cost of the opto-electronic components. The Phase-III CSAC incorporates a redesigned microwave synthesizer, with improved frequency resolution and provision for microprocessor control and optimization of the microwave power and, consequently, improved temperature performance and long-term stability. In addition, the firmware

has been rewritten to improve performance and robustness, implement auto-acquisition, and support internal and remote state-of-health determination.

PHYSICS PACKAGE DESIGN

Evolution of the physics package design from Phase-II to Phase-III is shown below in Figure 1.

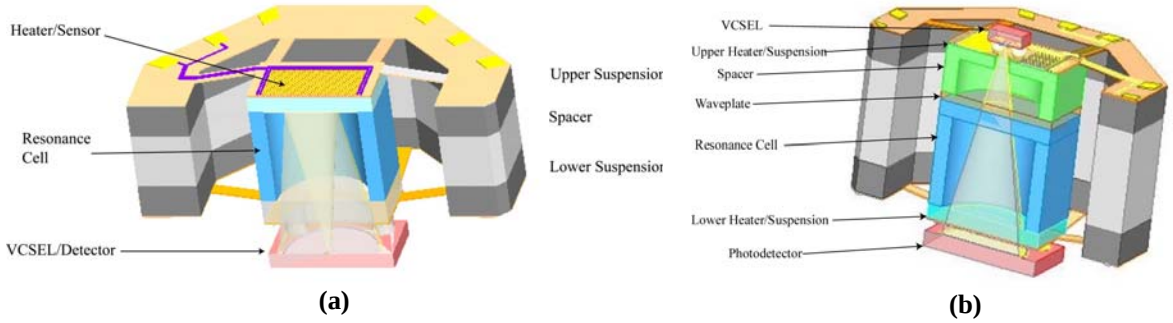


Figure 1. Physics package evolution from Phase-II (a) to Phase-III (b).

The Phase-III physics package (Figure 1(b), above) retains many of the successful features of the Phase-II design (from **[3]**, shown in Figure 1(a)). The heated resonance cell assembly is supported by tensioned polyimide "tethers," which provide extraordinary thermal isolation (7000°C/W) in a mechanically robust configuration. The electrical connections to the resonance cell assembly, as well as the heaters themselves, are patterned onto the polyimide, using conventional lithographic techniques, so that the dimensions of the (thermally conductive, metallic) traces are determined by electrical, rather than mechanical, requirements, thereby minimizing thermal losses through the electronic connections. The resonance cell itself, fabricated by anodic bonding of Pyrex® windows to a perforated silicon wafer, and containing a small amount of metallic cesium in addition to a temperature-compensating mixture of buffer gases, is also unchanged in the evolution from Phase-II to Phase-III.

The most significant departure from the Phase-II architecture is that the Phase-III physics package employs a "through-optical" path, rather than the "folded-optics" configuration of Phase-II. The advantage of the folded-optics approach, as described in **[3]**, is the minimization of the size of the resonance cell assembly, consequently reducing the suspended mass as well as the surface area for radiative heat loss. There are, however, several overwhelming disadvantages to this design, described below, which have led to the Phase-III architecture.

The Vertical-Cavity Surface Emitting Laser (VCSEL) is the most expensive component of the CSAC, due to its complex fabrication process and tight device specifications. While typical data communications VCSELs are relatively inexpensive, compared to conventional edge-emitting diode lasers, the CSAC requirements place unusual performance constraints on the device (see, for example, **[5]**), including frequency and polarization stability, low operating power and, perhaps most importantly, the requirement that the VCSEL wavelength be tuned to the 894.6 nm "D1" resonance of cesium at the cell operating temperature of 85°C. While most of the unusual VCSEL requirements can be accomplished by design, the yield of on-wavelength devices is limited by the uniformity of the epitaxial growth of the VCSEL structure. The Phase-II CSAC physics package incorporated a novel optoelectronic component in which a resonant-cavity photodiode (RCPD) was co-fabricated on the same substrate as the VCSEL. While this offers advantages in simplifying the component test and physics package assembly process, the VCSEL

itself occupies a relatively small area of the expensive gallium arsenide (GaAs) chip, thus increasing the chip cost significantly from the intrinsic limit.

As shown in Figure 2, the VCSEL wafer density has increased 16-fold by replacing the integrated VCSEL/RCPD device **(**a**)** with a standalone VCSEL device **(**b**)**. In addition, in the Phase-III design, two redundant VCSELs are fabricated on each chip. Independent electrical contacts to the two devices are provided via the four attachment pads, allowing VCSEL selection, subsequent to final assembly, from outside the vacuum-sealed physics package, thereby increasing top-level yield of functional physics packages. Further cost reduction is accomplished in the Phase-III design by replacing the GaAs photodiode with a conventional 1.5 mm diameter silicon photodiode.

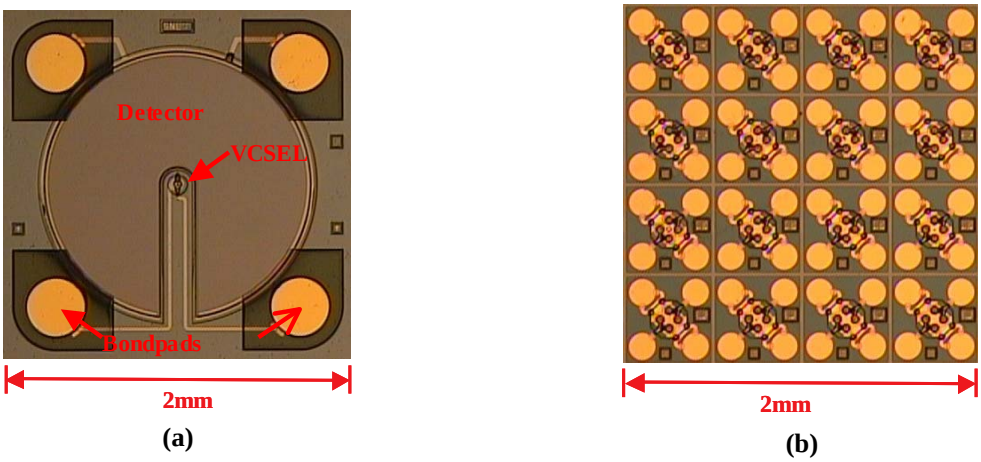
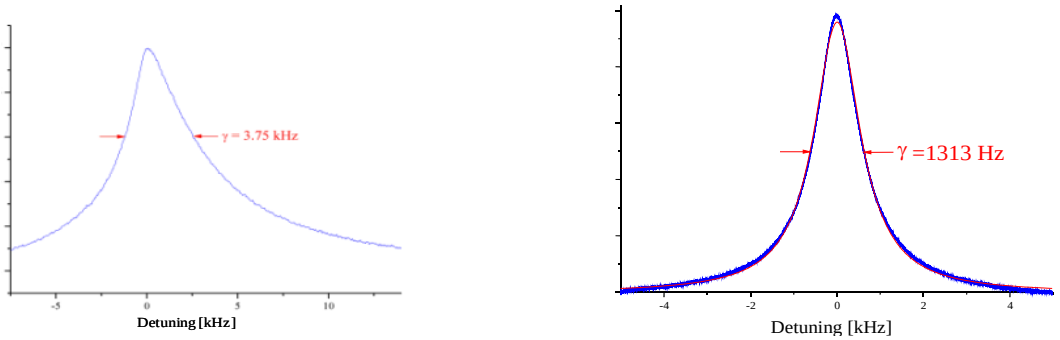


Figure 2. (a) Phase-II VCSEL/RCPD and (b) Phase-III VCSEL devices.

The Phase-III architecture also leads to a performance improvement over the Phase-II design, due to elimination of CPT lineshape asymmetry caused by the "inhomogeneous light shift." The optical intensity in the laser beam decreases as roughly $1/r^2$ with distance from the VCSEL aperture due to the natural divergence of the beam from an ≈5μm waist within the device. In the Phase-II design, the optical intensity experienced by the atoms at any point in the cell is determined by the sum of the intensities of the incident and retro-reflected beams. The geometry has been optimized, insofar as possible, to produce a uniform intensity distribution within the cell. Nonetheless, there are regions in the cell, particularly near the VCSEL aperture, where the intensity varies from the mean by as much as 1000X. The effect of the higher intensity is to shift the frequency of the CPT resonance towards higher frequencies due to the AC Stark effect ("light shift"). The composite lineshape, resulting from inhomogeneous averaging of the atomic resonance frequency over the entire cell volume, includes contributions from atoms experiencing all values of the intensity distribution. Fortunately, the number of atoms contained in the volume of the high-intensity cone near to the VCSEL aperture is small compared to the overall volume, which experiences a relatively uniform intensity distribution. Nonetheless, the inhomogeneous light shift creates an asymmetry and broadening of the CPT resonance, favoring higher frequencies, in proportion to the volume distribution of intensity in the cell.

The detrimental impact of the inhomogeneous light shift has been ameliorated in the Phase-III physics package architecture. The uniformity of the intensity distribution is improved by eliminating the folded optical path and by allowing distance for the laser beam to diverge before entering the cell. Determining the optimum length for the "spacer" (shown in green in Figure 1(b)) requires a system-level compromise

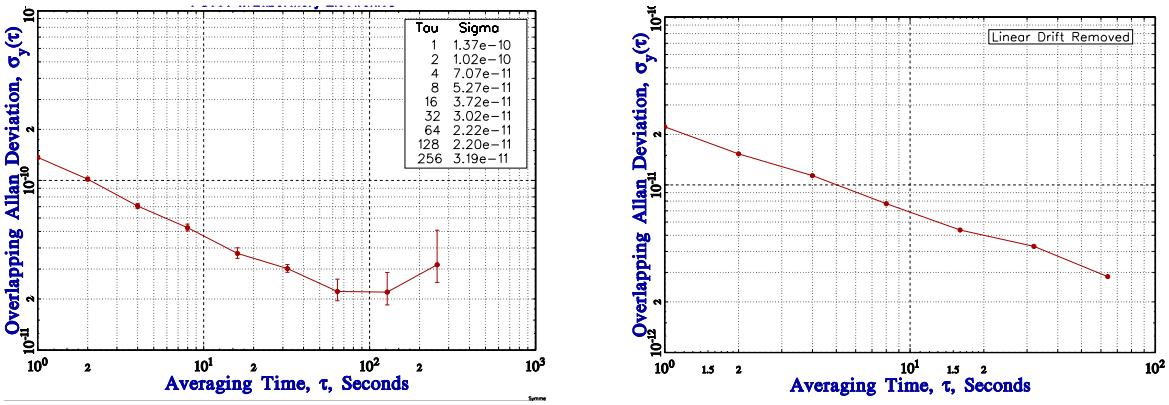
between (a) intensity uniformity and (b) the overall size of the physics package and the resulting additional power consumption due to the increase in surface area of the heated assembly. Numerical simulations and experiments were performed, early in the Phase-III development, to determine the optimum spacing. The optimized design, illustrated in Figure 1(b), results in an assembly that still fits, mechanically, within the existing vacuum package, consumes an additional 1-2 mW of heater power in a 25°C ambient, and results in considerable qualitative and quantitative improvement in the CPT resonance lineshape, as shown below in Figure 3.



(a) **(b)**

Figure 3. CPT resonance in (a) Phase-II and (b) Phase-III physics packages.

The Phase-II physics package CPT resonance, shown in Figure 3(a), is broadened and asymmetrically displaced towards higher frequencies due to the inhomogeneous light shift. The Phase-III resonance, in Figure 3(b), is nearly 3X narrower and nearly ideally Lorentzian. This improvement is expected to provide improved performance, both in the short-term and long-term stability of the CSAC.

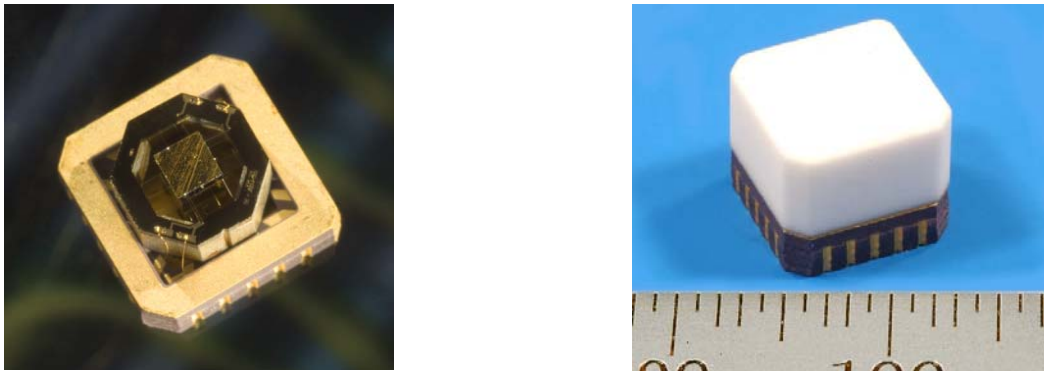


(a) **(b)**

Figure 4. Short-term frequency stability of (a) Phase-II and (b) Phase-III physics packages.

Figure 4, above, shows the short-term typical stability Allan deviation plots of **(**a**)** Phase-II and **(**b**)** Phase-III physics packages, each measured with optimized laboratory-scale electronic systems. As expected, the

short-term stability of the Phase-III physics package in improved by >3X, consistent with the linewidth reduction, compared to the Phase-II device, from $\sigma_y(\tau=1)\approx 1x10^{-10}$ to $\sigma_y(\tau=1)\approx 2x10^{-11}$.



(a) **(b)**

Figure 5. (a) Phase-III physics package in LCC and (b) sealed Phase-II physics package (Phase-III is similar).

Figure 5(a) shows a photograph of a Phase-III physics package (photodiode side up) mounted in the lower half of the vacuum package, a ceramic leadless chip carrier (LCC). Figure 5(b) is a photograph of a sealed Phase-II physics package, though the Phase-III device appears identical after vacuum sealing.

PHYSICS PACKAGE RELIABILITY

Excluding the physics package, the CSAC is comprised of conventional analog, digital, and microwave electronics, with well-understood performance and reliability specifications. The physics package itself, thus, constitutes the area of greatest uncertainty and risk to the production of a fieldable, reliable CSAC.

Vacuum Integrity

As shown in Figure 5 of Reference **[6]**, the thermal isolation of the resonance cell assembly is critically dependent on the vacuum pressure within the physics package. Below 10 mtorr, the physics package demands ≈10 mW of power to sustain the resonance cell temperature at 85°C. Above 10 mtorr, the power requirement rises rapidly to 70 mW at atmospheric pressure. Creating and sustaining sufficiently low vacuum pressure in the physics package requires careful selection of all internal components and adhesives from low-outgassing materials, clean handling, and careful attention to potential contaminants in processing, low-leakage sealing technique, and the inclusion of gettering material within the vacuum package. Development of the physics package at Draper Laboratory has included all of these, as well as the development of special-purpose vacuum sealing equipment that permits bakeout of the physics package assembly, activation of the getter, and sealing within a vacuum environment. Validation of the process can only be confirmed by long-term testing of vacuum integrity within the physics package.

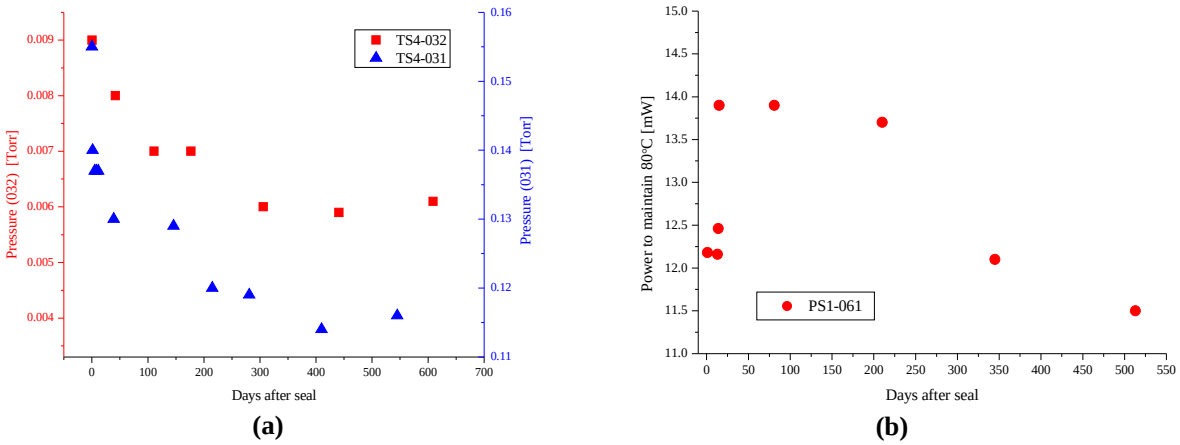


Figure 6. Vacuum aging of several devices (a) pressure vs. time and (b) power aging.

Several prototype physics packages were sealed early in the Phase-III development process and have been periodically monitored for degradation of vacuum. On two of the devices, the thermal response was calibrated for use as a pressure monitor in a vacuum bell jar prior to sealing. The subsequent vacuum performance of these two devices, designated TS4-031 and TS4-032, is shown in Figure 6(a). One device, TS4-031, had relatively high pressure, ≈160 mtorr, when initially sealed. Both devices, though, showed improvement in vacuum for at least the first 400 days and have not gotten significantly worse in 600 days of measurement. The third device, PS1-061, has been operated with a temperature controller for 500 days, with periodic monitoring of the required power to sustain 80°C. The data from this device are shown in Figure 6(b). This device also indicates no evidence of vacuum degradation 500 days after sealing. Combined, the data to date from these ongoing experiments indicate that the current design, process, and gettering material are capable of sustaining vacuum for at least 600 days.

Mechanical Integrity

The integrity of the polyimide suspension system, which provides mechanical support and thermal isolation for the resonance cell assembly, is critical to successful deployment of the CSAC. The fundamental resonances of the mechanical assembly have been calculated theoretically and compared to experimental measurements.

Experimentally, mechanical displacement of the resonance cell assembly is measured by laser rangefinding as variable frequency vibration is applied to the physics package. Figure 7(a) shows a typical response function as the drive frequency is varied across the mechanical resonance. In this case, the unit under test displays a fundamental resonance at ≈2 kHz with Q≈100. Figure 7(b) shows a comparison between theoretical mechanical models and experimental measurements of the resonance frequency as a function of the width and strain angle of the supporting tethers.

The resonance response of several devices was measured, both in air and vacuum, and compared to theoretical models.

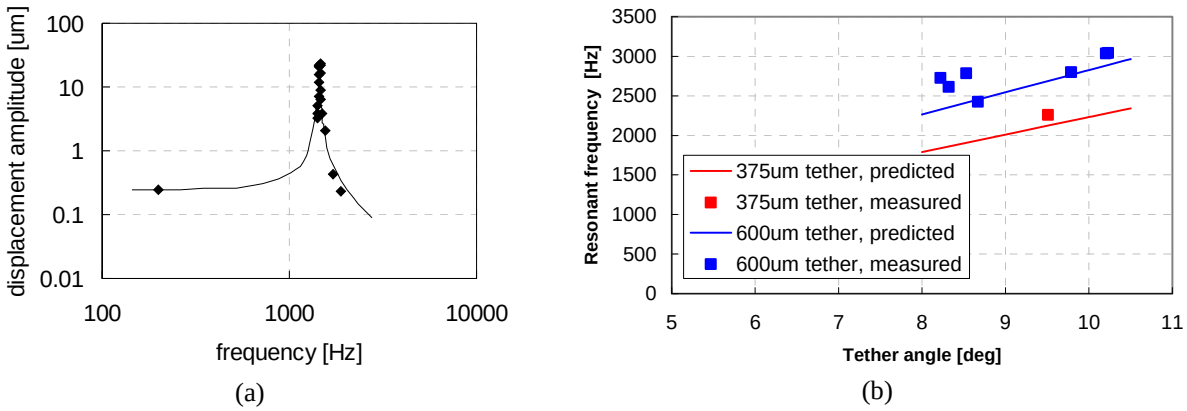


Figure 7. (a) Typical resonance response of physics package displacement and (b) comparison of measured resonant frequency with numerical predictions as a function of tether angle (strain) in two configurations.

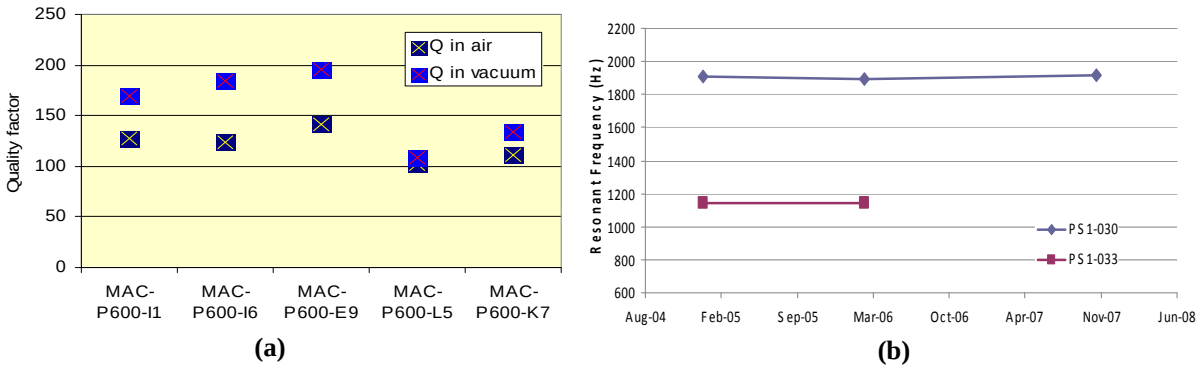


Figure 8. Resonance Q in air and vacuum for several devices.

Figure 8(a) shows the measured Q of the fundamental resonance, both in air and vacuum, of five sample devices. With these measurements, we have determined that the fundamental resonance in the Phase-III physics package occurs at approximately 2300 Hz and has a Q, in vacuum, of approximately 150.

In order to verify the long-term mechanical stability of the polyimide suspension design, the fundamental resonance of two devices was characterized early in the CSAC program and has been periodically measured. Figure 8(b) shows the long-term drift of the mechanical resonant frequency of two prototype CSAC suspensions, measured over nearly 3 years. Unfortunately, one device, PS1-033 was irreparably damaged due to mishandling in removing it from the test fixture following the March 2006 evaluation. Nonetheless, the results from these two devices indicate no discernable degradation of the polyimide support system after 3 years of storage.

Shock testing has been performed on Phase-III physics packages, in order to further evaluate mechanical robustness. Seven devices were fabricated, by standard assembly procedures, but incorporating off-wavelength VCSELs (in order to preserve on-wavelength VCSEL inventory). Each device was subjected to shock along four axes: **x**, **xy**, **+z**, and **–z**, as defined in Figure 9, below.

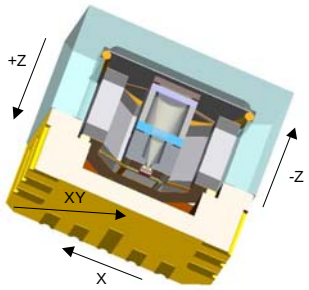


Figure 9. Definition of physics package principal axes for shock testing.

Each device was subjected to three half-sine shock pulses, along each of the four axes, of progressively increasing amplitude, from 50 to 1000g, according to the procedures of MIL-STD 202G. Following each sequence of three pulses, each device was subjected to full electrical functionality testing. All devices displayed full functionality following shock of 500g along all axes. Two of the seven devices were only tested to 500g maximum shock pulse. Of the other five devices, all showed failure of one or more polyimide tethers at 1000g along one of the four axes.

Initially, the results of the shock testing were in conflict with our theoretical models, which predict that the Phase-III physics package should sustain strain in excess of 1000g without damage. Subsequent Fourier analysis has indicated that the standard 0.5 ms 1000g half-sine shock pulse contains sufficient energy at the mechanical resonance frequency of the test devices (2500 to 3000 Hz) to induce an equivalent static force of 1600g. This is in better agreement with the predicted shock failure level.

Experiments are ongoing to improve our understanding of the limitations of the polyimide strain limit and to improve the shock survivability. Nonetheless, together with the mechanical displacement measurements, which indicate a fundamental resonance at > 2 kHz, these results confirm the fundamental robustness and suitability of the CSAC architecture, as well as the validity of our theoretical mechanical models.

VCSEL Reliability

One of the greatest concerns, at the outset of the CSAC program, was the reliability of the Vertical Cavity Surface Emitting Laser (VCSEL). The reliability of VCSEL devices is well-understood and literally millions of VCSELs have been deployed worldwide in applications ranging from telecommunications transmitters to computer mice. The CSAC is a particularly demanding application for VCSELs for several reasons **[5]**: First, the VCSEL must be temperature stabilized at the resonance-cell temperature, 85°C, to stabilize its wavelength. Second, the requirement for single-transverse-mode operation leads to relatively small emitting aperture and correspondingly high current density in the active region. Both of these lead to degradation of the expected functional lifetime of the VCSEL, compared to room-temperature operation of more conventional large-aperture devices.

The custom VCSEL devices for this project were developed at Sandia National Laboratories. In order to estimate the projected lifetime, a controlled lifetest was conducted at Sandia. Forty devices were tested under accelerated life conditions, including elevated temperature and current density, in order to induce failures and thereby predict lifetime under “normal” CSAC operating conditions. Sample results are shown below in Figure 10.

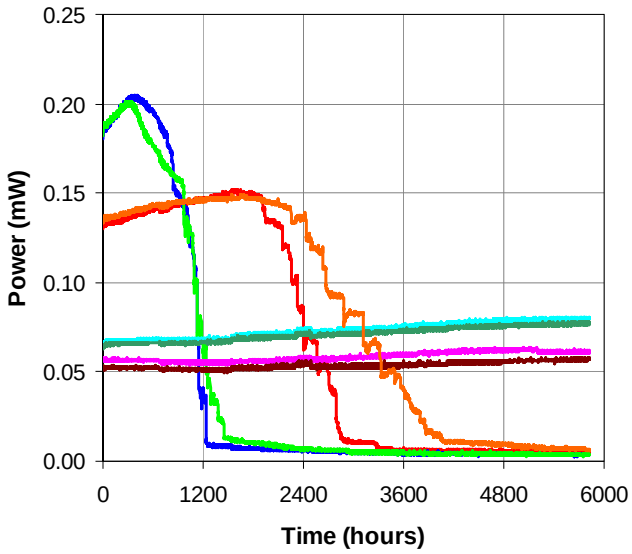


Figure 10. VCSEL accelerated lifetest results.

The results of the VCSEL life test are quite encouraging. Following 10 months of accelerated aging, the results from orthogonal test conditions consistently predict a mean time to failure (MTTF) of > 10 years under CSAC operating conditions, well in excess of the expected mission life for CSAC-enabled handheld battery-powered instruments.

PHYSICS PACKAGE PERFORMANCE

Nearly 20 Phase-III physics packages were fabricated for the pre-production build of 10 CSACs. Figure 11 shows the collected short-term Allan deviation measurements for 10 devices, again measured with optimized laboratory electronics, along with the CSAC project objective of $\sigma_y(\tau=1)<6x10^{-10}$. All of the Phase-III physics packages exhibit STS of $\sigma_y(\tau=1)<6x10^{-11}$, 10X margin beyond our design goals.

ELECTRONIC DESIGN

The CSAC electronic design has been described extensively in Reference **[4]**. The electronic control systems remained largely unchanged in preparation for the CSAC pre-production build. The most significant changes were in the redesign of the microwave synthesizer and the operating firmware, which are discussed below.

Microwave Synthesizer

In the Phase-II prototype, described in Reference **[4]**, the microwave synthesizer consisted of a 4.6 GHz voltage-controlled oscillator (VCO), which was phase-locked to a 20.0 MHz temperature-compensated crystal oscillator (TCXO) via a commercially available low-power dual-modulus integer PLL. This synthesizer enabled the CSAC to provide a standard RF frequency, 20.0 MHz ± 1 part in 10^8, with phase noise determined by the TCXO, rather than the VCO. For interrogation of the atomic resonance, modulation was applied within the PLL loop filter, thus avoiding the detrimental impact of modulation appearing on the TCXO output. For the Phase-III pre-production build, it was desired to improve the microwave synthesizer to provide (a) precise digital calibration of the output frequency to the full level of

precision of the CSAC; (b) pure square-wave frequency modulation at 4.6 GHz; and (c) microprocessor control and optimization of the microwave power amplitude applied to the physics package.

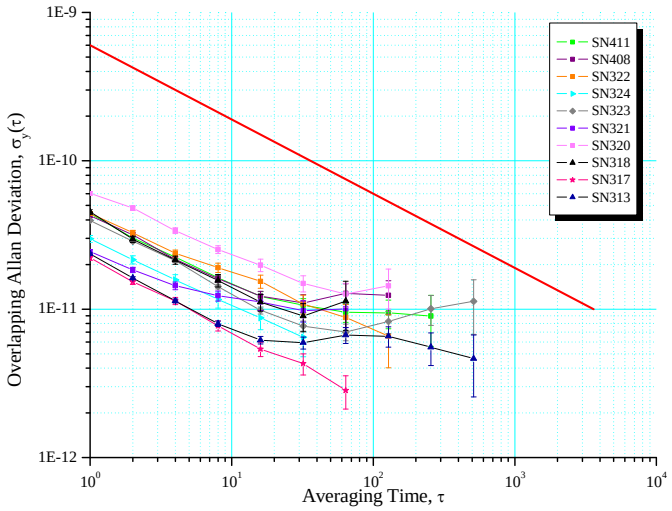


Figure 11. Short-term frequency stability of 10 Phase-III physics packages. CSAC performance objective of $\sigma_y(\tau=1)<6x10^{-10}$ is shown in red.

The objectives above appeared impossible, within the CSAC power and size budget, at the outset of the CSAC program. Fortunately, though, the commercial cellular telephone market has driven the development of low-power microwave synthesizers that are nearly ideal for the CSAC application. Recently, low-power fractional-N PLL devices have become available that enable precise synthesis of microwave frequencies up to 6 GHz.

Figure 12(a) shows a block diagram of the Phase-III microwave synthesizer. As in the Phase-II design, the synthesizer consists of a 4.6 GHz VCO phase-locked to a TCXO. In the Phase-III design, the TCXO output is at 10.0 MHz and the relative tuning between the TCXO and VCO may be digitally controlled with a resolution of 2 parts in 10^{12}. Square-wave frequency modulation is applied directly to the VCO via microprocessor control of the PLL. A PIN diode attenuator has been implemented at the synthesizer output, permitting microprocessor control of the microwave power over a range of 15 dB. Figure 12(b) shows the single-sideband (SSB) phase noise of the 10.0 MHz output under normal CSAC operating conditions. The action of the main clock servo is evident at the clock servo bandwidth of 100 Hz. At offset frequencies above the 100 Hz clock servo bandwidth, the phase noise reflects the intrinsic phase noise of the TCXO. Below 100 Hz, the phase noise reflects the stability of the CSAC physics package.

FIRMWARE ALGORITHMS

The fundamental firmware algorithms were largely unchanged between the original Phase-II CSAC demonstration and the Phase-III pre-production build. However, the original firmware was largely comprised of *ad hoc* experimental software code that was difficult to maintain and debug. The firmware was rewritten for Phase-III, using modern structured code practices. An additional servo algorithm was developed to optimize and stabilize the microwave power to the atomic resonance, via the microwave synthesizer attenuator control. Internal monitoring of critical control parameters was implemented, along with alarm indicators and a telemetry interface for monitor and control of the CSAC. Finally, algorithms

were developed for automated turn-on and initial acquisition of optimum tuning parameters for the cell temperature, laser current control, microwave power control, and frequency output.

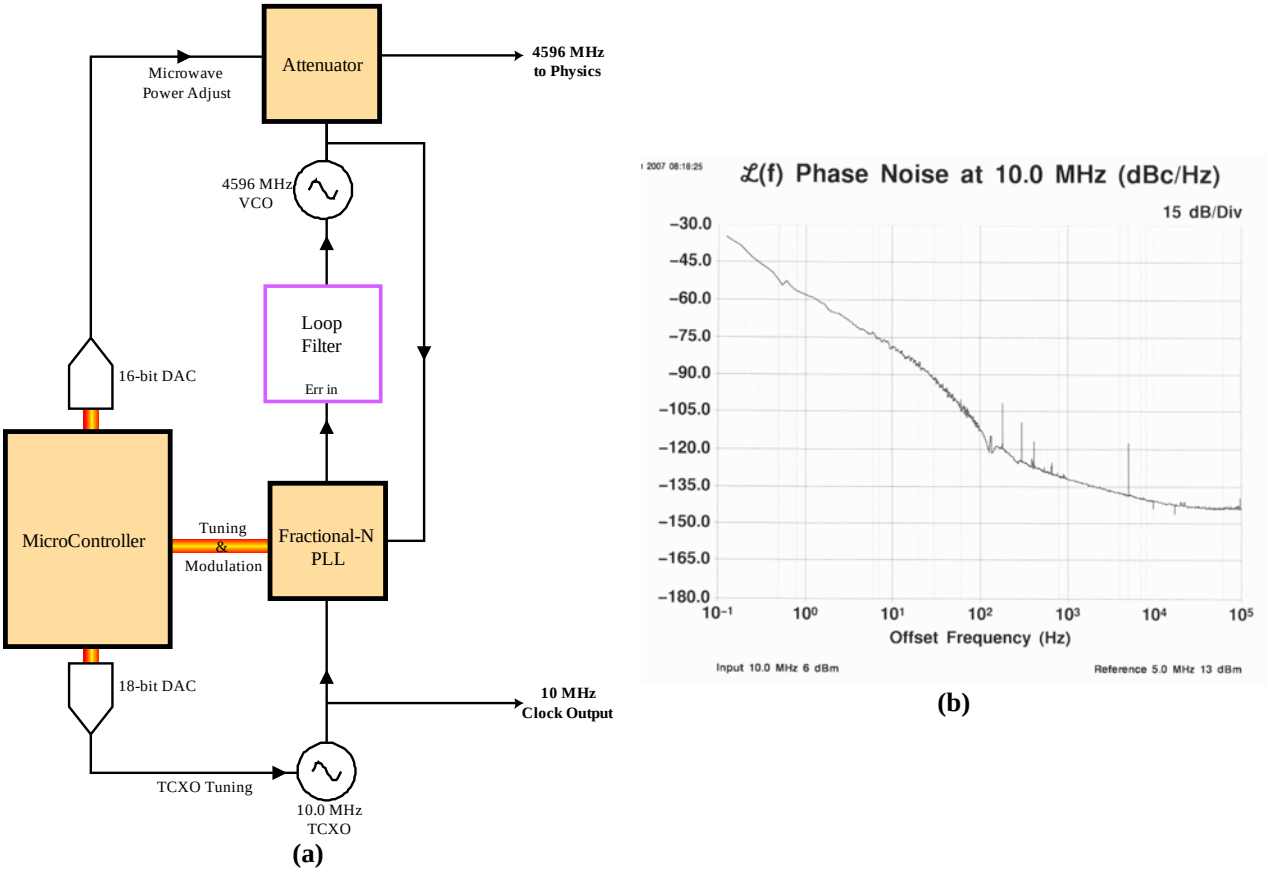


Figure 12. (a) Block diagram of the CSAC microwave synthesizer and (b) SSB phase noise of 10.0 MHz output.

Figure 13 shows a typical acquisition sequence, as observed via the CSAC telemetry interface. The entire acquisition sequence, from a cold start in a 25°C ambient, takes a little over 2 minutes. Approximately the first 110 seconds are spent waiting for the physics package to thermally stabilize, prior to the onset of servo acquisition. Once the heaters have stabilized, the four main servos, for the laser wavelength, laser power, microwave power, and TCXO frequency, are sequentially initiated, after which lock is declared and the clock outputs are enabled. The acquisition time could be reduced considerably by allowing for higher demand power to the heater circuits, though this would increase the overall power budget for the CSAC.

CSAC PERFORMANCE

In total, nearly 20 Phase-III CSACs were constructed, in various configurations for engineering and testing purposes. The “pre-production build” consists of 10 nearly identical devices that were subjected to a standard protocol of acceptance tests. Many of these have since been delivered to DoD organizations

for evaluation and systems demonstrations. The remainder of this paper summarizes experimental test results on the pre-production CSAC devices.

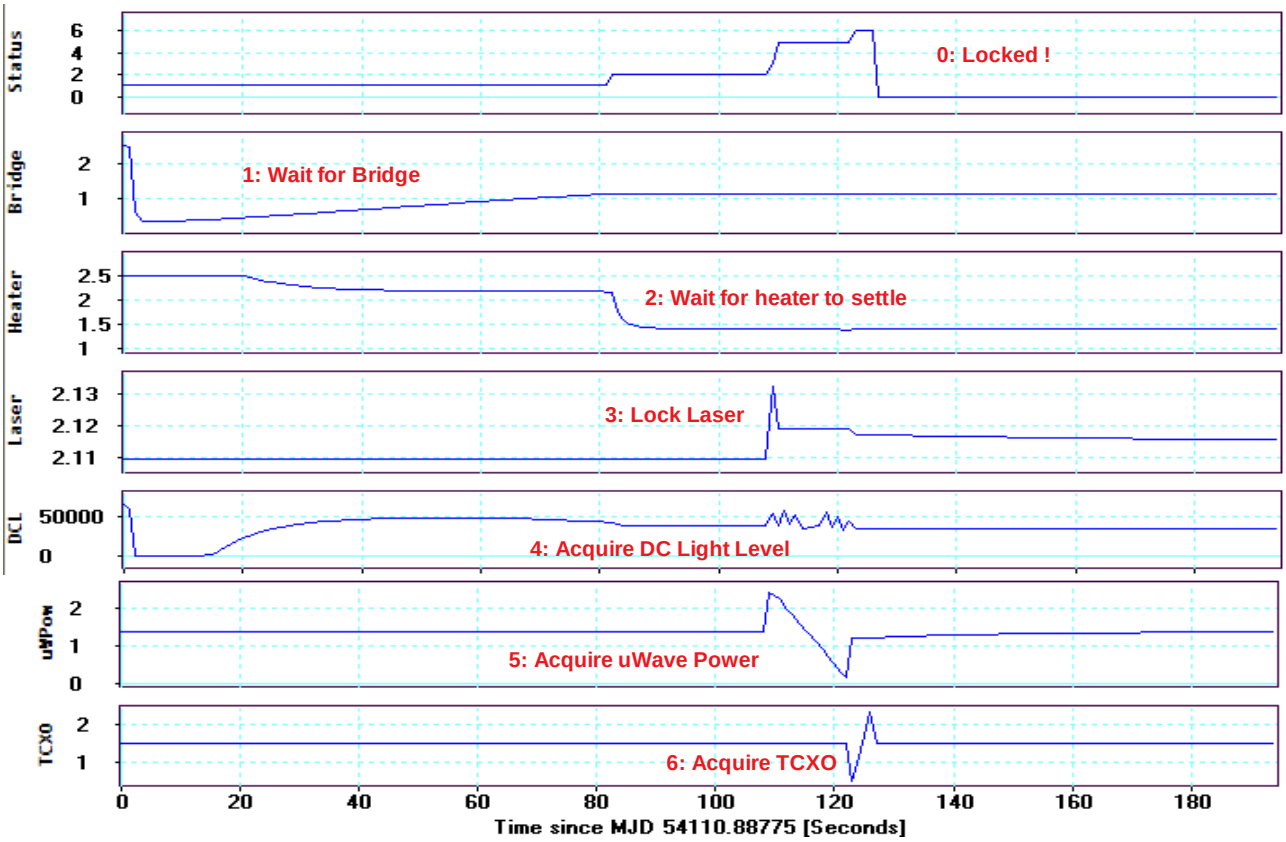


Figure 13. CSAC acquisition sequence.

SHORT-TERM STABILITY

Figure 14 shows the short-term stability of 10 pre-production CSACs. The data on each device were taken immediately following initial calibration. As a result, the units are "green" and the frequency drift is relatively high, typically $dy/dt \approx 10^{-10}$/day, which impacts the medium-term stability (beyond 10^3 seconds). Over all 10 units the average short-term stability is $\sigma_y(\tau=1)=1.6\times10^{-10}$, nearly 4X margin over the project goal of $\sigma_y(\tau=1)<6\times10^{-10}$. The relative performance of the CSACs is well correlated with the independent measurements of physics package performance (see Figure 11), though the performance is generally degraded by 3X, compared to that of the laboratory electronics used for the physics package characterization, principally due to the inferior phase noise performance of the low-power CSAC synthesizer.

LONG-TERM STABILITY

One device, SN084, was constructed early in Phase-III and set aside for long-term monitoring of frequency.

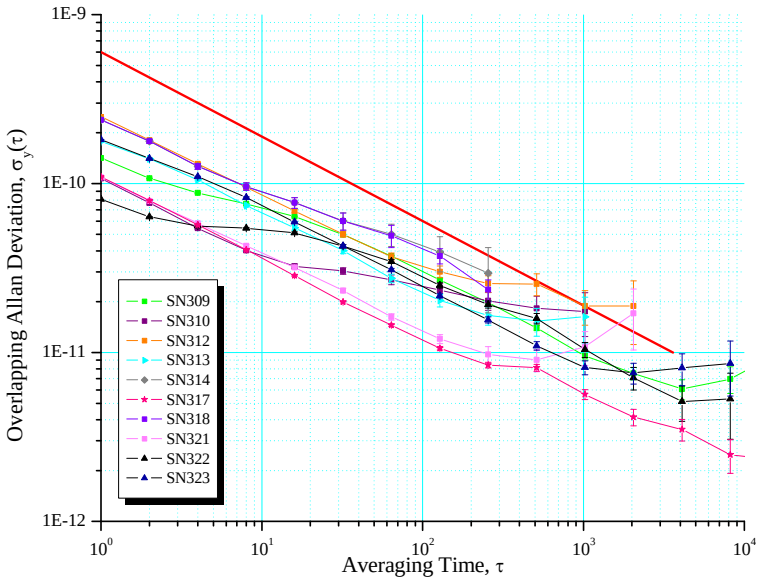


Figure 14: Short-term stability of 10 pre-production CSACs

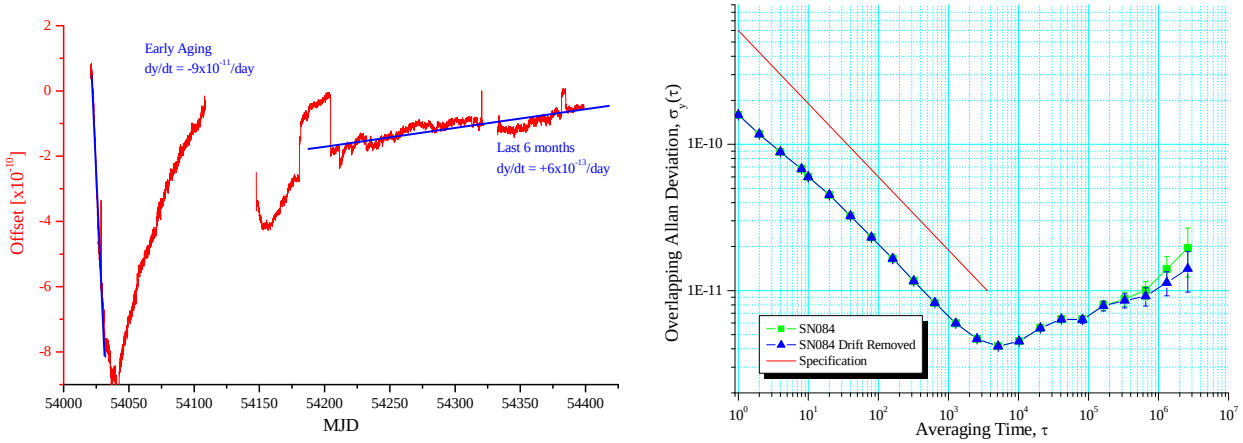


Figure 15. Long-term aging data of CSAC SN084: (a) frequency and (b) stability of last 6 months.

Figure 15(a) is a 1-year frequency record for SN084. There are several steps and restarts in the data due to various measurement equipment failures. In addition, the unit was removed on MJD 54108-54148 for firmware and electronics upgrades. Nonetheless, the frequency aging performance of the unit is evident. Early after assembly, for the first 2-3 weeks, the unit evidenced a large negative frequency aging. Following this early equilibration period, the sign of the frequency drift changed to positive. Within a month, the amplitude of the drift was below 10^{-11}/day. After 6 months of aging, the drift was below 10^{-12}/day. Figure 15(b) shows the Allan deviation of SN084, computed on the second half of the dataset in Figure 15(a), i.e. for 6 months of data following 6 months of initial aging. The Allan deviation is

calculated both with the linear component of drift removed (in blue) and without (in green). There is little difference between the two within 10^6 seconds, indicating that the frequency "flicker" floor is dominated by other effects, such as the temperature sensitivity of the CSAC.

PERFORMANCE OVER TEMPERATURE

In real world applications, the CSAC may be subjected to temperature variations of ± 10°C and most require qualification over a range of ΔT=0-50°C, or wider. In extreme temperature applications, the key parameters are power consumption and frequency change with temperature.

Because of the extraordinary thermal isolation of the physics package, the power consumption of the CSAC is relatively insensitive to ambient temperature, compared to conventional atomic clocks. At lower operating temperatures, the physics package requires slightly more heater power (roughly 1 mW/7°C), but other components, such as the microprocessor, run more efficiently. The upper temperature limit is determined by the requirement to temperature-stabilize the physics package at ≈85°C. Even with the heaters turned off, the VCSEL dissipates ≈2mW, which limits the upper operating ambient to ≈70°C.

Figure 16, below, shows the CSAC power consumption as a function of ambient temperature. It is not surprising that the power consumption decreases by several milliwatts at elevated ambient from 40-70°C. It is surprising, though, that the power is also reduced at lower temperatures, indicating that the power savings of cooling the other electronic components offsets the increased heater power required by the physics package. In general, the power consumption changes by only 1-2%, from the nominal 125 mW, over the nominal operating range of 0-50°C.

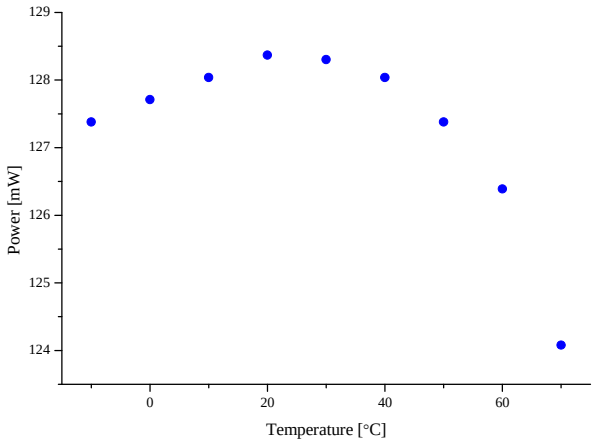


Figure 16. CSAC Power Consumption vs. Ambient Temperature.

The frequency change of the CSAC over temperature is caused by several different and interacting sources that affect the frequency of the cesium CPT resonance. The principal sources of CPT temperature coefficient are changes in the buffer gas and the laser spectrum which impact the collisional shift and AC Stark shift, respectively. In order to reduce the effects of the buffer gas collisions, the resonance cell is filled with a mixture of two buffer gases, argon and nitrogen, which produce oppositely signed shifts of the resonance line (-191 Hz/torr and +924 Hz/torr, respectively) **[13]**. Spectral variations are minimized, insofar as possible, by the servos, which stabilize the DC power of the VCSEL and optimize the microwave modulation amplitude. Nonetheless, there remains some temperature coefficient in the CSAC, due to second-order buffer gas effects, spectral changes due to thermal gradients in the physics

package (which change the DC bias point of the VCSEL), and other electronic effects, such as variation of the magnetic bias field circuit. The Phase-III CSAC typically displays a nearly linear frequency response to changes in ambient temperature, as shown below in Figure 17.

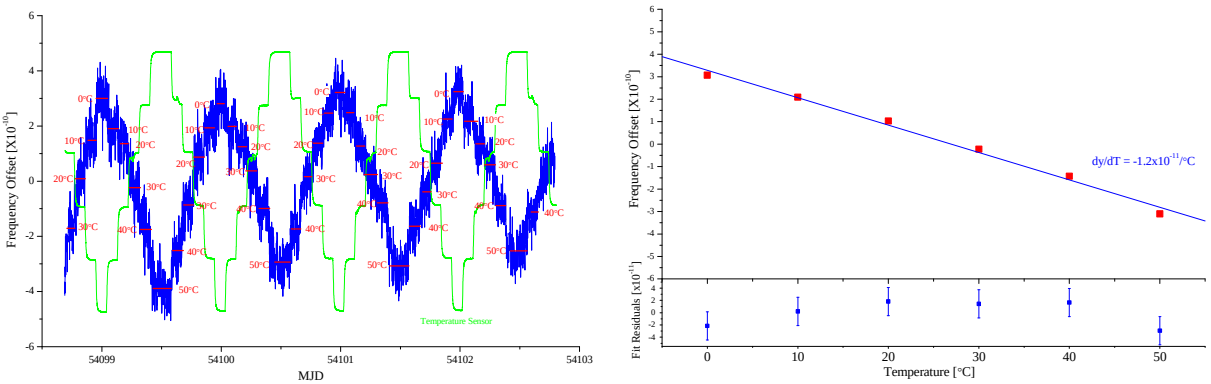


Figure 17. Frequency sensitivity to temperature: (a) red labels indicate temperature, blue is CSAC frequency error, and green is internal sensor reading; (b) Frequency vs. Temperature from (a) red is data and blue is linear fit (dy/dT=-1.2x10^{-11}/°C); lower plot shows fit residuals.

Figure 17(a) shows the typical temperature sensitivity of one of the pre-production CSACs. In this case, CSAC SN310 was placed in a temperature chamber. The chamber was stepped, in 10°C steps, from 0°C to 50°C, with a 2-hour dwell at each point. The frequency offset of the CSAC (in blue) was measured while the reading from the internal temperature sensor (on the CSAC circuit board) was recorded via RS232 telemetry (shown in green). Figure 17(b) shows the average of the repetitive frequency readings plotted against the chamber temperature. The temperature response is nearly linear, as evidenced by the quality of the linear fit, dy/dt=-1.2x10^{-11}/°C, shown in blue. The plot residuals, in the bottom trace of Figure 17(b) exhibit peak-to-peak variation of ≈5x10^{-11}, more than an order of magnitude lower than the temperature coefficient.

The monotonic and nearly linear temperature coefficient, along with its high degree of correlation with the internal temperature sensor, suggests the possibility that the temperature coefficient of the CSAC could be improved considerably via microprocessor compensation using the digital synthesizer tuning.

Figure 18 displays the dramatic improvement possible with digital compensation. The data of Figure 17(a) are reproduced on the left of Figure 18(a). Unit SN310 was subsequently removed from the temperature chamber and digital compensation was implemented. The compensated performance is shown on the right of Figure 18(a).

Digital compensation was implemented in all of the pre-production CSACs. Figure 18(b) shows the collected 0-50°C temperature coefficient for 10 of the CSACs, without compensation (red) and with compensation enabled (blue). Uncompensated, most behave similarly to Figure 17(a), with temperature-driven frequency errors in the range of $\Delta y/\Delta T \approx 1\text{-}4\times10^{-9}$/50°C. Figure 18(b) shows that the compensation works fairly well for most units, reducing the temperature coefficient to $\Delta y/\Delta T < 5\times10^{-10}$/50°C. For several units, the correlation between the uncompensated frequency change and the onboard temperature sensor is relatively poor, so that the compensation provides little, if any improvement. One unit in particular, SN309, exhibits poor symmetry between up-going temperature changes and down-going temperature

changes, perhaps reflecting a thermal discontinuity within the physics package. Nonetheless, the average temperature coefficient for the 10 units shown in Figure 18(b) is $\Delta y/\Delta T = 3 \times 10^{-10}/50°C$.

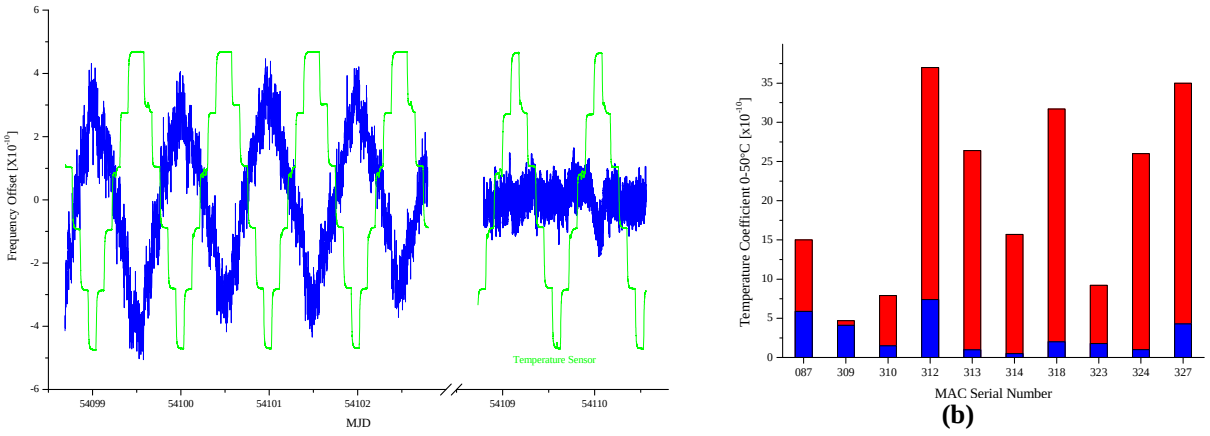


Figure 18. (a) Temperature sensitivity without compensation (left) and with compensation enabled (right); (b) temperature coefficient (0-50°C) for 10 CSACs both with compensation enabled and disabled.

PERFORMANCE UNDER VIBRATION

The impact of random vibration on CSAC performance was measured on one unit, SN309. The CSAC was mounted on a vibration table in three orientations: x, y, and z, where z is the principal axis of the physics package and x and y are two orthogonal axes. Short-term stability and phase noise of the CSAC 10 MHz output was monitored as the CSAC was subjected to a 10 Hz to 2 kHz random vibration profile at levels ranging from 0.7 to 3.0 g RMS.

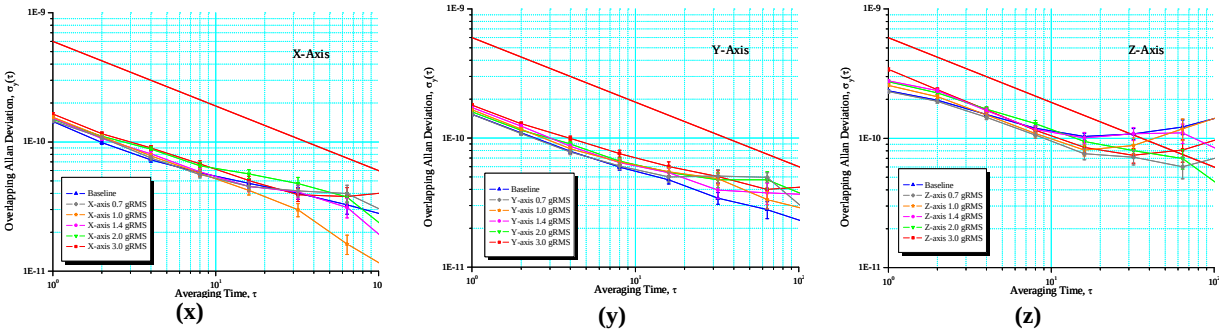


Figure 19. Impact of vibration along (x), (y), and (z) axes on short-term stability.

Figure 19 shows the impact of random vibration on the short-term stability of CSAC SN309 at varying levels and directed along each of the principal axes, **x**, **y**, and **z**. Each plot also includes a "baseline" measurement (in blue) in which the CSAC was mounted on the shaker and the drive coils were energized, but no vibration was applied. Along each axis, the short-term stability performance was degraded by

< 10% at the highest test level (3 g RMS). Note that the **z**-axis performance was degraded, even at baseline, due to the 8 Gauss magnetic field of the shaker.

TOWARDS A 1 CM^3, 30 MW CSAC

The Phase-III CSAC, as described herein, has a volume of ≈15 cm^3 and consumes roughly 125 mW of power. As a field-deployable device, this CSAC will provide atomic timing performance for a host of portable battery-powered applications, enabling secure access to communication networks, and advanced PNT systems. Nonetheless, at 125 mW, the power consumption remains relatively high for battery-powered timing applications, particularly for the clock, which must remain powered continuously, even when the system is otherwise in a power-conserving "sleep" mode. Of somewhat lesser criticality, but still of value to systems integrators, is the further reduction in the size of the CSAC, particularly in applications where the CSAC is being retrofitted into existing systems, in the space heretofore occupied by miniature TCXOs.

While developing production capability for the Phase-III CSAC remains our highest priority, in order to provide deployable CSACs for critical DoD applications, we continue research and development of smaller lower-power CSACs. We anticipate that, as the design evolves in the laboratory, power and size improvements will be introduced into production in an evolutionary fashion.

POWER CONSUMPTION

The power budget for the 125 mW CSAC is detailed below in Table 1.

Table 1. CSAC power budget.

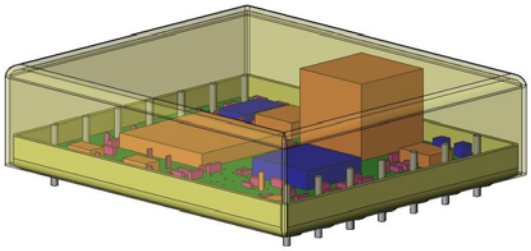
System	Component	Power
Signal Processing	MicroController	20 mW
	16-Bit DACs	13 mW
	Analog	8 mW
Physics	Heater Power	7 mW
	VCSEL Power	3 mW
	C-Field	1 mW
Microwave/RF	4.6 GHz VCO	32 mW
	PLL	20 mW
	10 MHz TCXO	7 mW
	Output Buffer	1 mW
Power Regulation & Passive Losses		13 mW
Total		125 mW

A cursory review of Table 1 provides direction for CSAC power reduction. Nearly half of the total power, 60 mW, is consumed by the microwave synthesizer. The microprocessor subsystem consumes nearly 40 mW and an additional 13 mW is dissipated in the power regulator circuits.

VOLUME

For simplicity of development, construction, and debugging, little effort was made to reduce the volume of the Phase-III CSAC. The entire CSAC, including the physics package, are assembled onto one single-

sided printed-circuit board (PCB).



Physics Package	1.0 cm^3
C-Field Coil	0.4 cm^3
Active components	0.9 cm^3
Passive components	0.2 cm^3
PCB	1.3 cm^3
Mu-Metal housing	2.3 mm^3
Empty Space	10.0 cm^3
Total	**16 cm^3**

(a) **(b)**

Figure 20. (a) Phase-III solid model and (b) volume composition.

The Phase-III CSAC, as illustrated in Figure 20(a) and tabulated in Figure 20(b) leaves considerable room for improvement. In the current 16 cm^3 design, nearly 2/3 of the volume, 10 cm^3, is occupied by empty space. A straightforward repackaging effort, utilizing multiple double-sided PCBs and smaller passive components, could reduce the volume to 2-3 cm^3. Achieving the 1 cm^3 goal will require size reduction of the physics package as well as a higher degree of electronic integration, including the development of application-specific integrated circuits.

1 CC, 30 MW PROTOTYPE

For demonstration purposes, we have built a 1 cm^3, 30 mW CSAC prototype. An essential component of this demonstration was the reduction of the physics package volume, as shown below in Figure 21.

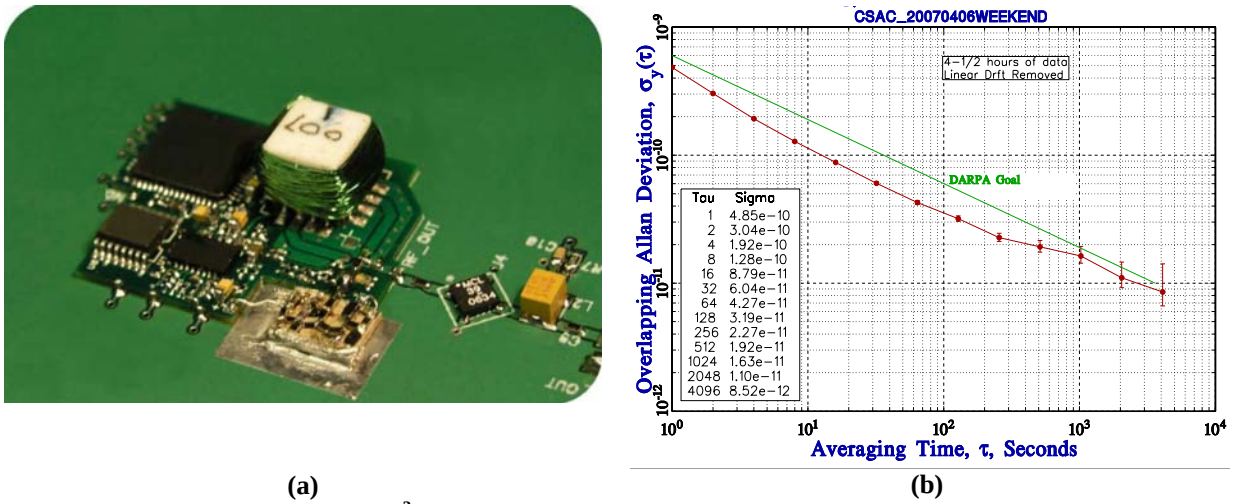
(a) **(b)**

Figure 21. (a) Solid models of original 1 cm^3 physics package and 0.35 cm^3 miniature physics package; (b) photos of same.

As shown in the solid model of Figure 21(a), the polyimide suspensions were redesigned to eliminate empty vacuum space, but the dimensions of the resonance cell assembly were not modified in order to preserve the performance of the physics package. Unused electrical feedthroughs were eliminated with

the selection of a smaller ceramic LCC and vacuum lid. Overall, the volume of the vacuum-sealed physics package assembly was reduced from 1 cm^3 to 0.35 cm^3, nearly a 3X volume reduction.

In order to reduce the power consumption, it was necessary to eliminate the PLL and TCXO from the microwave synthesizer. It was a highly ambitious task to develop a suitably low-noise microwave oscillator to support the CSAC performance goals without synthesizing from the low-noise TCXO. A low-phase-noise 4.6 GHz oscillator, based on a thin-film resonator (TFR), was developed in collaboration with Spectral Research **[7]**. Instead of locking the TCXO to the CPT signal, via the microwave synthesizer, the TFR oscillator was locked directly to the atomic resonance. The consequences of this architecture are that the user output, from the CSAC, is at the "natural" atomic frequency of 4.635 GHz, the frequency output cannot be calibrated, the interrogation square wave frequency modulation is present on the output signal, and we are unable to implement digital temperature compensation. The advantages are significant reductions in power, size, and complexity. Additional power reduction was accomplished by eliminating internal voltage regulation, minimizing the demand power of the heater circuit, and by taking advantage of low-power "sleep" modes of the microprocessor.



(a) **(b)**

Figure 22. (a) The 1 cm^3, 30 mW CSAC demonstration and (b) ADEV measurement.

Figure 22(a) shows a photograph of the miniature ultralow-power CSAC demonstration prototype. The total volume of the prototype is 0.95 cm^3, calculated from the volume of the components and PCB, assuming measurement by water displacement. The total power consumption was measured to be 29.5 mW. Figure 22(b) shows an Allan deviation measurement of the frequency stability of the 4.6 GHz CSAC output, which was divided by 304, using externally-powered electronic dividers, to 15.3 MHz for comparison with the Symmetricom 10 MHz master clock.

In this configuration, the CSAC cannot be conveniently integrated into existing applications, which typically require 10.0 MHz calibrated output. Moreover, in reducing the power consumption of the CSAC, additional burden is placed on the host system, which not only must accommodate a 4.6 GHz uncalibrated reference signal contaminated by modulation sidebands, but also must provide low-noise regulated 2.6 VDC and magnetic shielding for the CSAC. Nonetheless, this is an important demonstration of the possibilities for future CSAC evolution. Already, some of the innovations of this demonstration, such as the 0.35 cm^3 physics package and the low-power microprocessor operation, are being incorporated into the production CSAC design.

CONCLUSIONS

We have completed the development of a 125 mW, 15 cm^3 CSAC, based on the original CSAC prototype design previously presented at PTTI 2005. We have evolved the design to improve short- and long-term frequency stability and manufacturability and have completed firmware design to support autonomous acquisition and operation in field-deployable systems. We have presented results of reliability testing of the physics package, including VCSEL lifetime, vacuum aging, mechanical aging of the suspension, and shock survival. We have built 10 "pre-production" CSACs and have verified consistent short-term stability and temperature performance. We have also presented initial results for long-term stability and drift, vibration sensitivity, and power consumption over temperature. In a laboratory configuration, we have demonstrated a 1 cm^3, 30 mW CSAC prototype.

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